Claims

What is claimed is:

1	1. A Complementary Metal Oxide Semiconductor (CMOS) bi-directional
2	current mode differential link comprising:
3	a CMOS driver receiving a data input and having an output coupled
4	to a transmission line;
5	a CMOS replica driver receiving said data input and providing a
6	replica driver output substantially equal to said CMOS driver output;
7	a CMOS receiver coupled to both said transmission line and replica
8	driver output; said CMOS receiver comprising a resistor summing network
9	and a differential amplifier; and
10	said CMOS driver and said CMOS replica driver including a plurality
11	of parallel current sources; each of said current sources being arranged to
12	send positive or negative current through a load responsive to an applied
13	control signal.
1	2. The CMOS bi-directional current mode differential link of Claim 1,
2	wherein said resistor summing network comprises:
3	a first resistor, a first end of said first resistor being coupled to a
4	positive phase output node of said CMOS driver;
5	a second resistor, a first end of said second resistor being coupled to a
6	second end of said first resistor, and a second end of said second resistor
7	being coupled to a negative phase output of said replica driver;
8	a third resistor, a first end of said third resistor being coupled to a
9	negative phase output of said CMOS driver; and

10	a fourth resistor, a first end of said fourth resistor being coupled to a		
11	second end of said third resistor, and a second end of said fourth resistor		
12	being coupled to a positive phase output of said replica driver.		
1	3. The CMOS bi-directional current mode differential link of Claim 2,		
2	wherein said differential amplifier comprises:		
3	a first input coupled to a first node comprising said second end of said first		
4	resistor and said first end of said second resistor; and		
5	a second input coupled to a second node comprising said second end of said		
6	third resistor and said first end of said fourth resistor.		
1	4. The CMOS bi-directional current mode differential link of Claim 2,		
2	wherein said first resistor, said second resistor, said third resistor, and		
3	said fourth resistor are each of resistance magnitude at least ten times the		
4	characteristic impedance of said transmission line.		
1	5. The CMOS bi-directional current mode differential link of Claim 2,		
2	further comprising:		
3	a first capacitor, a first end of said first capacitor being coupled to said first		
4	input of said differential amplifier, and a second end of said first capacitor		
5	being coupled to ground; and		
6	a second capacitor; a first end of said second capacitor being coupled to said		
7	second input of said differential amplifier, and a second end of said second		
8	capacitor being coupled to ground.		
1	6. The CMOS bi-directional current mode differential link of Claim 2,		
2	wherein at least one of said first, second, third, and fourth resistors is split		
3	into a plurality of series-connected resistors, each coupling of two of said		
4	series-connected resistors defining an inter-resistor node.		

1	7.	The CMOS bi-directional current mode differential link of Claim 6,
2		wherein at least one instant node of said inter-resistor nodes is further
3		coupled to a first end of an inter-resistor capacitor instance unique to the
4		instant node, and where a second end of each said inter-resistor capacitor
5		instance is coupled to ground.
1	8.	A method of receiving signals in a CMOS bi-directional current mode
2		differential link, wherein said link comprises a data driver receiving a
3		data input and having an output coupled to a first end of a transmission
4		line; a replica driver receiving said data input and providing a replica
5		driver output substantially equal to said data driver output; a receiver
6		comprising a resistor-summing network and a differential amplifier; and
7		said data driver and said replica driver including a plurality of parallel
8		current sources; each of said current sources in said plurality of current
9		sources being arranged to send positive or negative current through a load
10		responsive to an applied control signal; said receiver capable of receiving
11		a signal sent from a similar link coupled to a second end of said
12		transmission line; said method comprising the steps of:
13		coupling a positive phase output of said data driver to a first end of a first
14		resistor in said resistor-summing network;
15		coupling a second end of said first resistor to a first input of said
16		differential amplifier, and further coupling said second end of said first
17		resistor to a first end of a second resistor in said resistor-summing
18		network;
19		coupling a second end of said second resistor to a negative phase output
20		of said replica driver;
21		coupling a negative phase output of said data driver to a first end of a
22		third resistor in said resistor-summing network;
44		and resistor in said resistor-summing network,

23	coupling a second end of said third resistor to a second input of said
24	differential amplifier, and further coupling said second end of said third
25	resistor to a first end of a fourth resistor in said resistor-summing
26	network; and
27	coupling a second end of said fourth resistor to a positive phase output of
28	said replica driver.
1	9. The method of Claim 8, further comprising the step of splitting at least
2	one of said first, second, third, and fourth resistors into two or more
3	series-coupled resistors; each coupling of series-coupled resistors
4	constituting an instance of an inter-resistor node.
1	10. The method of Claim 8, further comprising the step of coupling a first
2	end of a first capacitor to said first input of said differential amplifier; and
3	coupling a second end of said first capacitor to ground.
1	11. The method of Claim 8, further comprising the step of coupling a first
2	end of a second capacitor to said second input of said differential
3	amplifier; and coupling a second end of said second capacitor to ground.
1	12. The method of Claim 9, further comprising the step of coupling a first
2	end of an instance capacitor to at least one instant node of said inter-
3	resistor nodes, said instance capacitor being unique to each said inter-
4	resistor node; and coupling a second end of each said instance capacitor
5	to ground.